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| EXAMINER | |
|---|---|
| GEIB, BENJAMIN P | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/616,647 | HUANG ET AL. | |
| | Examiner | Art Unit | |
| | BENJAMIN P. GEIB | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20 and 22-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment received 01/28/2008.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-20 and 22-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Regarding claims 1 and 19, the claims recite the limitations “verifying whether the thread control ID” [emphasis added] and “a match between the thread control ID” [emphasis added]. These limitations render the claims indefinite as it is unclear which of the previously mentioned thread control IDs is being referenced. For the remainder of the examination, "the thread control ID" recited in the above-cited limitations will be interpreted as "the thread control ID associated with the thread control element” as it appears to be what applicant intended and clarifies which thread control ID is being referenced.

### *Allowable Subject Matter*

5. Claims 1-20 and 22-28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art, including the disclosures of Arnold et al. (U.S. Patent No. 6,438,681), Shiell et al. (U.S. Patent No. 5,913,049), Hirata et al. (U.S. Patent No. 5,430,851), and Hirata et al. (“An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads”), alone or combination have not taught or render obvious the recited comparing, verifying, and prohibiting associated with a thread control

ID (in combination with all other limitations of the independent claims). These features are recited via the following limitations of independent claims 1 and 19:

(Claim 1)

"comparing, with a comparator, a thread control ID associated with the thread control element with pipeline thread control IDs in a pipeline";

"verifying whether the thread control ID matches any pipeline thread control IDs";

"in response to ... a match between the thread control ID and a pipeline thread control ID, prohibiting the instruction held in the corresponding thread control element form executing in that clock cycle"

(Claim 19)

"comparing a thread control ID associated with the thread control element with pipeline thread control IDs in a pipeline";

"verifying whether the thread control ID matches a pipeline thread control ID";

"in response to … a match between the thread control ID and the pipeline thread control ID, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle"';

7. Claims 2-18 and 20, 22-28 depend from claims 1 and 19, respectively, and are considered allowable for at least the reasons indicated for claims 1 and 19.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 29-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Arnold et al., U.S. Patent No. 6438,681 (Hereinafter Arnold).

10. Referring to claim 29, Arnold has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions *[register stage circuitry; See FIG. 3] [The register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47]*, wherein said thread control elements are not part of a pipeline stage or pipeline storage location *[the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)]*;

a set of one or more comparing elements *[comparison logic; FIG. 3, component 24]*, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements *[column 6, lines 50-66]*; and

a set of one or more temporary register identification pipeline storage locations *[latches; FIG. 3, components 89, 91, and 93]*, wherein the one or more temporary register identification pipeline storage locations are directly coupled to the one or more comparing elements *[column 6, lines 50-66]*.

11. Referring to claim 30, Arnold has taught the system of claim 29, further comprising an instruction buffer *[latch (FIG. 3, component 58)]* coupled to the one or more thread control elements *[column 6, lines 35-49]*.

12. Referring to claim 31, Arnold has taught the system of claim 30, further comprising an arbiter *[instruction dispersal unit; FIG. 1, component 18]*, wherein the arbiter is coupled to the one or more thread control elements, the one or more comparing elements, and the one or more temporary register identification pipeline storage locations *[See FIGs. 1 & 3; column 3, lines 13-23]*.

13. Referring to claim 32, Arnold has taught the system of claim 31, further comprising an arithmetic logic unit (ALU) *[pipeline; FIGs. 1 & 3, component 21]* coupled to the arbiter *[column 3, lines 13-32]*.

14. Referring to claim 33, Arnold has taught the system of claim 32, further comprising a set of one or more input data buffers *[latch (FIG. 3, component 58)]* coupled to the arbiter, wherein each input data buffer corresponds to a thread control element of the one or more thread control elements *[column 6, lines 35-49]*.

15. Referring to claim 34, Arnold has taught the system of claim 33, further comprising a set of one or more temporary register buffers *[the registers that are identified by the register identifiers]* coupled to the arbiter, wherein each temporary register buffer corresponds to a thread control element of the one or more thread control elements *[column 6, lines 35-49]*.

16. Referring to claim 35, Arnold has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions *[register stage circuitry; See FIG. 3] [The register stage processing circuitry receives instructions from the instruction dispersal unit; column 3, lines 13-23, 44-47]* wherein said thread control elements are not part of a pipeline stage or storage location *[the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)]*;

a set of one or more comparing elements *[comparison logic; FIG. 3, component 24]*, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements and wherein each thread control element and comparing element forms a bi-directional correspondence *[column 6, lines 50-66]*;

a set of one or more temporary register identification pipeline storage locations *[latches; FIG. 3, components 89, 91, and 93]*, wherein the one or more temporary register pipeline storage locations are directly coupled to the one or more comparing elements *[See FIG. 3; column 6, lines 50-66]*, and

an arbiter *[instruction dispersal unit; FIG. 1, component 18]* coupled to the thread control elements, the comparing elements, and the temporary register pipeline storage locations in each stage of a pipeline or pipelines *[See FIGs. 1 & 3; column 3, lines 13-23]*.

***Response to Arguments***

17. Applicant's arguments with respect to claim 29-34 have been fully considered but they are not persuasive.

18. Applicant argues the rejection/novelty of claims 29-34, in substance, that:

> "Arnold fails to disclose, teach or suggest the highlighted features in claim 29 above." [i.e. "wherein said thread control elements are not part of a pipeline stage or pipeline storage location"] (Pages 18-19)
>
> "Arnold fails to disclose teach or suggest the highlighted features in claim 35 above." ["a set of one or more thread control elements for fetching instructions wherein said thread control elements are not part of a pipeline stage or storage location"] (Pages 20-21)

19. These arguments are not found persuasive for the following reasons.

Regarding the Applicant's argument that Arnold has not taught "wherein said thread control elements are not part of a pipeline stage or pipeline storage location" (and similar limitation in claim 35), the Applicant asserts that "the Examiner improperly attempts to partition the register stage 25 and processing circuitry 66 from the rest of the pipeline 21". The examiner disagrees. The register stage circuitry (i.e. thread control element) is outside of the temporary register identification pipeline storage locations (See FIG. 3) and is, therefore, "not part of a pipeline stage or pipeline storage locations". That is, the Applicant has not specified what pipeline stage or storage location that the thread control element is not part of and, since the register stage circuitry is not part of the temporary register identification pipeline, the register stage circuitry is not part of a pipeline stage.

***Conclusion***

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hirata et al. (U.S. Patent No. 5,430,851) and Hirata et al. ("An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads") have taught a processor with multiple simultaneous threads that checks for dependencies among instructions.

Shiell et al. (U.S. Patent No. 5,913,049) has taught a processor with multiple simultaneous streams that includes dependency check logic.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BPG/

Benjamin P Geib
Examiner
Art Unit 2181

/Tonia LM Dollinger/
Primary Examiner, Art Unit 2181